HY11P14
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 4x40 LCD Driver
Low Noise Amplifier
18-Bit ΣΔADC

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目錄

注意：

1、 本說明書中的內容，隨著產品的改進，有可能不經過預告而更改。請客戶及時到本公司網站下載更新 http://www.hycontek.com

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4、 請注意輸入電壓、輸出電壓、負載電流的使用條件，使 IC 內的功耗不超過封裝的容許功耗。對於客戶在超出說明書中規定額定值使用產品，即使是瞬間的使用，由此所造成的損失，本公司不承擔任何責任。

5、 本產品雖內置防靜電保護電路，但請不要施加超過保護電路性能的過大靜電。

6、 本規格書中的產品，未經書面許可，不可使用在要求高可靠性的電路中。例如健康醫療器械、防災器械、車輛器械、車載器械及航空器械等對人體產生影響的器械或裝置，不得作為其部件使用。

7、 本公司一直致力於提高產品的品質和可靠度，但所有的半導體產品都有一定的失效概率，這些失效概率可能會導致一些人身事故、火災事故等。當設計產品時，請充分留意冗餘設計，採用安全指標，這樣可以避免事故的發生。

8、 本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特點

- 8 位元加強型精簡指令集，共有 66 個指令包含硬體乘法指令及查表指令
- 2.2V to 3.6V工作電壓範圍，-40℃~85℃工作溫度範圍
- 外部石英震盪器及內部高精度 RC 震盪器，6 種 CPU 工作時脈切換選擇，可讓使用者達到最佳省電規劃
  - 運行模式 300uA@2MHz
  - 待機模式 3uA@32KHz
  - 休眠模式 1uA
- 8KWord OTP (One Time Programmable) Type 程式記憶體，512Byte 資料記憶體
- Brownout and Watch dog Timer，可防止 CPU 進入死機模式
- 18bit 全差動輸入 ΣΔADC 類比數位轉換器
  - 內置 PGA (Programmable Gain Amplifier) 及可有 1/4、1/2、1. .....128 倍 10 種輸入信號放大倍率選擇
  - 內置輸入零點調整，可針對不同應用增加其量測範圍
  - 內置高阻抗輸入緩衝器(4 以上輸入倍率不適用)
  - 內置絕對溫度感測器
- 超低輸入雜訊(<1uVpp)運算放大器，可提供高輸出阻抗小訊號的放大及小電流的電壓轉換
- 1.0V, 1.2V 的內部類比電路共地電壓源，具有 Push-Pull 驅動能力，可提供傳感器驅動電壓
- LVD 低電壓檢測功能具 14 段檢測電壓設置與外部輸入電壓檢測功能
- 類比電壓源 VDDA 可選擇 4 種不同輸出電壓，具 10mA 穩壓電壓源輸出能力
- 4x40 LCD 液晶驅動器
  - Static、1/2、1/3、1/4 Duty 及 1/3 Bias 軟體選擇
  - 內建 Charge Pump 穩壓線路，提供 4 種 LCD 偏壓
- 增強型比較器
  - 兩組電壓源產生器
  - 具 0.25 倍或 0.5 倍工作電壓比較與自動轉態功能及 15 段比較電壓設置
  - 內置溫度感測電路
- 8-bit Timer A
- 16-bit Timer B 模組具 Capture/Compare 功能
- 8-bit Timer C 模組具 PWM/PFD 波形產生功能
- 串列通訊 SPI、EUART 模組
- Support 8 stack level

2. 引腳定義

2.1 LQFP100 引腳圖

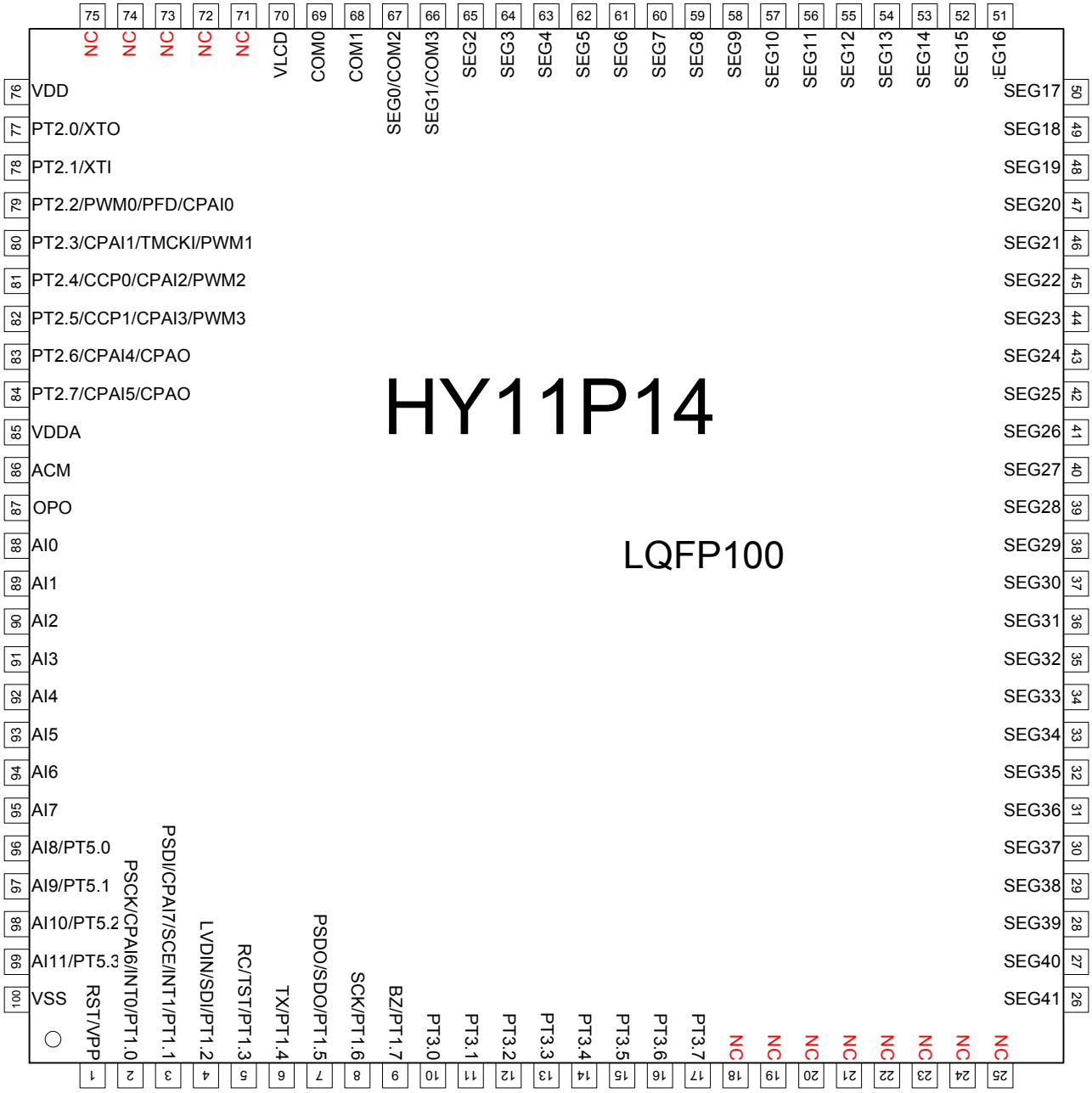


圖 2-1 HY11P14 LQFP100 引腳圖

2.2 LQFP64 引腳圖

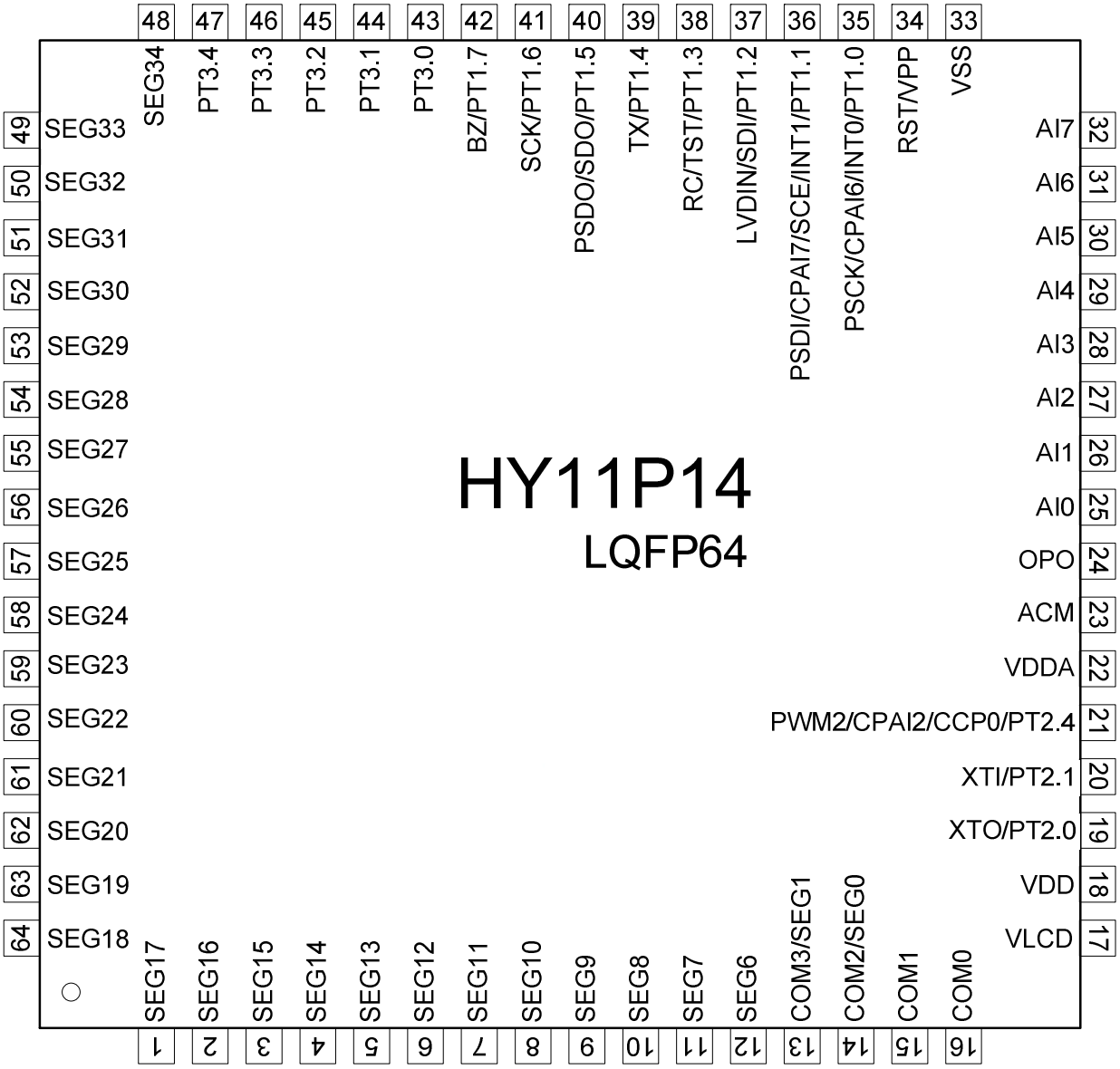


圖 2-2 HY11P14 LQFP64 引腳圖

註 1：VPP與RST復用同一接口，非燒錄EPROM時禁止輸入電壓超過 5.8V

註 2：TST與PT1.3 復用同一接口，操作時禁止輸入電壓超過VDD+0.3V

註 3：若不將PT1.3 設定成外部引腳按鍵，可以提升抗干擾能力

2.3 I/O引腳定義

"I/O"輸入/輸出,"I"輸入,"O"輸出,"S"史密斯觸發,"C"CMOS特性兼容輸出與輸入,"P"電壓源,"A"類比通道

LQFP64 引腳編號	LQFP100 引腳編號	引腳名稱	引腳特性		功能說明
			格式	緩衝	
34	1	RST/VPP			
		RST	I	S	復位晶片
		VPP	P	P	EPROM 讀/寫時的電壓源
35	2	PT1.0/INT0/PSCK/CPAI6			
		PT1.0	I	S	數位輸入
		INT0	I	S	中斷源 INT0
		PSCK	I	S	OTP 讀/寫介面 SCK 接口
		CPAI6	I	A	ECPA 類比輸入通道
36	3	PT1.1/INT1/PSDI/SCE/CPAI7			
		PT1.1	I	S	數位輸入
		INT1	I	S	中斷源 INT1
		PSDI	I	S	OTP 讀/寫介面 SDI 接口
		SCE	I/O	S	SPI 通訊介面 SCE 接口
		CPAI7	I	A	ECPA 類比輸入通道
37	4	PT1.2/SDI/LVDIN			
		PT1.2	I	S	數位輸入
		SDI	I/O	S	SPI 通訊介面 SDI 接口
		LVDIN	A	A	LVD 外部信號輸入接口
38	5	PT1.3/TST/RC			
		PT1.3	I	S	數位輸入
		RC	I	S	EUART 通訊介面 RC 接口
		TST	I	S	測試模式致能輸入（未開放）
39	6	PT1.4/TX			
		PT1.4	I/O	S	數位輸入/輸出
		TX	I/O	S	EUART 通訊介面 TX 接口
40	7	PT1.5/PSDO/SDO			
		PT1.5	I/O	S	數位輸入/輸出
		PSDO	O	C	OTP 讀/寫介面 SDO 接口
		SDO	I/O	S	SPI 通訊介面 SDO 接口
41	8	PT1.6/SCK			
		PT1.6	I/O	S	數位輸入/輸出
		SCK	I/O	S	SPI 通訊介面 SCK 接口
42	9	PT1.7/BZ			

		PT1.7 BZ	I/O O	S C	數位輸入/輸出 蜂鳴器輸出端
43	10	PT3.0	I/O	C	數位輸入/輸出
44	11	PT3.1	I/O	C	數位輸入/輸出
45	12	PT3.2	I/O	C	數位輸入/輸出
46	13	PT3.3	I/O	C	數位輸入/輸出
47	14	PT3.4	I/O	C	數位輸入/輸出
-	15	PT3.5	I/O	C	數位輸入/輸出
-	16	PT3.6	I/O	C	數位輸入/輸出
-	17	PT3.7	I/O	C	數位輸入/輸出
-	18	NC	-	-	未使用
-	19	NC	-	-	未使用
-	20	NC	-	-	未使用
-	21	NC	-	-	未使用
-	22	NC	-	-	未使用
-	23	NC	-	-	未使用
-	24	NC	-	-	未使用
-	25	NC	-	-	未使用
-	26	SEG41	O	A	LCD 的 Segment 輸出
-	27	SEG40	O	A	LCD 的 Segment 輸出
-	28	SEG39	O	A	LCD 的 Segment 輸出
-	29	SEG38	O	A	LCD 的 Segment 輸出
-	30	SEG37	O	A	LCD 的 Segment 輸出
-	31	SEG36	O	A	LCD 的 Segment 輸出
-	32	SEG35	O	A	LCD 的 Segment 輸出
48	33	SEG34	O	A	LCD 的 Segment 輸出
49	34	SEG33	O	A	LCD 的 Segment 輸出
50	35	SEG32	O	A	LCD 的 Segment 輸出
51	36	SEG31	O	A	LCD 的 Segment 輸出
52	37	SEG30	O	A	LCD 的 Segment 輸出
53	38	SEG29	O	A	LCD 的 Segment 輸出
54	39	SEG28	O	A	LCD 的 Segment 輸出
55	40	SEG27	O	A	LCD 的 Segment 輸出
56	41	SEG26	O	A	LCD 的 Segment 輸出
57	42	SEG25	O	A	LCD 的 Segment 輸出
58	43	SEG24	O	A	LCD 的 Segment 輸出
59	44	SEG23	O	A	LCD 的 Segment 輸出

60	45	SEG22	O	A	LCD 的 Segment 輸出
61	46	SEG21	O	A	LCD 的 Segment 輸出
62	47	SEG20	O	A	LCD 的 Segment 輸出
63	48	SEG19	O	A	LCD 的 Segment 輸出
64	49	SEG18	O	A	LCD 的 Segment 輸出
1	50	SEG17	O	A	LCD 的 Segment 輸出
2	51	SEG16	O	A	LCD 的 Segment 輸出
3	52	SEG15	O	A	LCD 的 Segment 輸出
4	53	SEG14	O	A	LCD 的 Segment 輸出
5	54	SEG13	O	A	LCD 的 Segment 輸出
6	55	SEG12	O	A	LCD 的 Segment 輸出
7	56	SEG11	O	A	LCD 的 Segment 輸出
8	57	SEG10	O	A	LCD 的 Segment 輸出
9	58	SEG9	O	A	LCD 的 Segment 輸出
10	59	SEG8	O	A	LCD 的 Segment 輸出
11	60	SEG7	O	A	LCD 的 Segment 輸出
-	61	SEG6	O	A	LCD 的 Segment 輸出
-	62	SEG5	O	A	LCD 的 Segment 輸出
-	63	SEG4	O	A	LCD 的 Segment 輸出
-	64	SEG3	O	A	LCD 的 Segment 輸出
-	65	SEG2	O	A	LCD 的 Segment 輸出
13	66	COM3/SEG1	O	A	LCD 的 COM 與 Segment 共用輸出
14	67	COM2/SEG0	O	A	LCD 的 COM 與 Segment 共用輸出
15	68	COM1	O	A	LCD 的 COM 輸出
16	69	COM0	O	A	LCD 的 COM 輸出
17	70	VLCD	P	P	LCD 的電壓源
-	71	NC	-	-	未使用
-	72	NC	-	-	未使用
-	73	NC	-	-	未使用
-	74	NC	-	-	未使用
-	75	NC	-	-	未使用
18	76	VDD	P	P	晶片工作電壓源
19	77	PT2.0/XTO PT2.0 XTO	I/O A	S A	數位輸入/輸出 外接振盪器輸出端

20	78	PT2.1/XTI			
		PT2.1	I/O	S	數位輸入/輸出
		XTI	A	A	外接振盪器輸入端
-	79	PT2.2/PWM0/PFD/CPAI0			
		PT2.2	I/O	C	數位輸入/輸出
		PWM0	O	C	PWM 輸出接口
		PFD	O	C	PFD 輸出接口
		CPAI0	I	A	ECPA 類比輸入通道
-	80	PT2.3/TMCKI/CPAI1/PWM1			
		PT2.3	I/O	S	數位輸入/輸出
		TMCKI	I	S	TIMERC 時脈源輸入接口
		CPAI1	I	A	ECPA 類比輸入通道
		PWM1	O	C	PWM 輸出接口
21	81	PT2.4/CCP0/CPAI2/PWM2			
		PT2.4	I/O	S	數位輸入/輸出
		CCP0	I	S	捕捉/比較模式信號接口
		CPAI2	I	A	ECPA 類比輸入通道
		PWM2	O	C	PWM 輸出接口
-	82	PT2.5/CCP1/CPAI3/PWM3			
		PT2.5	I/O	S	數位輸入/輸出
		CCP1	I	S	捕捉/比較模式信號接口
		CPAI3	I	A	ECPA 類比輸入通道
		PWM3	O	C	PWM 輸出接口
-	83	PT2.6/CPAI4/CPAO			
		PT2.6	I/O	C	數位輸入/輸出
		CPAI4	I	A	ECPA 類比輸入通道
		CPAO	I	A	ECPA 比較器輸出接口
-	84	PT2.7/CPAI5/CPAO			
		PT2.7	I/O	C	數位輸入/輸出
		CPAI5	I	A	ECPA 類比輸入通道
		CPAO	I	A	ECPA 比較器輸出接口
22	85	VDDA	P	P	穩壓器輸出，類比電路電壓源
23	86	ACM	P	P	內部類比電路共地引腳
24	87	OPO	A	A	運算放大器輸出
25	88	AI0	A	A	類比輸入通道
26	89	AI1	A	A	類比輸入通道
27	90	AI2	A	A	類比輸入通道
28	91	AI3	A	A	類比輸入通道

29	92	AI4	A	A	類比輸入通道
30	93	AI5	A	A	類比輸入通道
31	94	AI6	A	A	類比輸入通道
32	95	AI7	A	A	類比輸入通道
-	96	PT5.0/AI8 PT5.0 AI8	 I A	 C A	 數位輸入 類比輸入通道
-	97	PT5.1/AI9 PT5.1 AI9	 I A	 C A	 數位輸入 類比輸入通道
-	98	PT5.2/AI10 PT5.2 AI10	 I A	 C A	 數位輸入 類比輸入通道
-	99	PT5.3/AI11 PT5.3 AI11	 I A	 C A	 數位輸入 類比輸入通道
33	100	VSS	P	P	晶片工作電壓源接地端

表 2-1 引腳定義與功能說明

3. 應用電路

3.1 橋式感測器

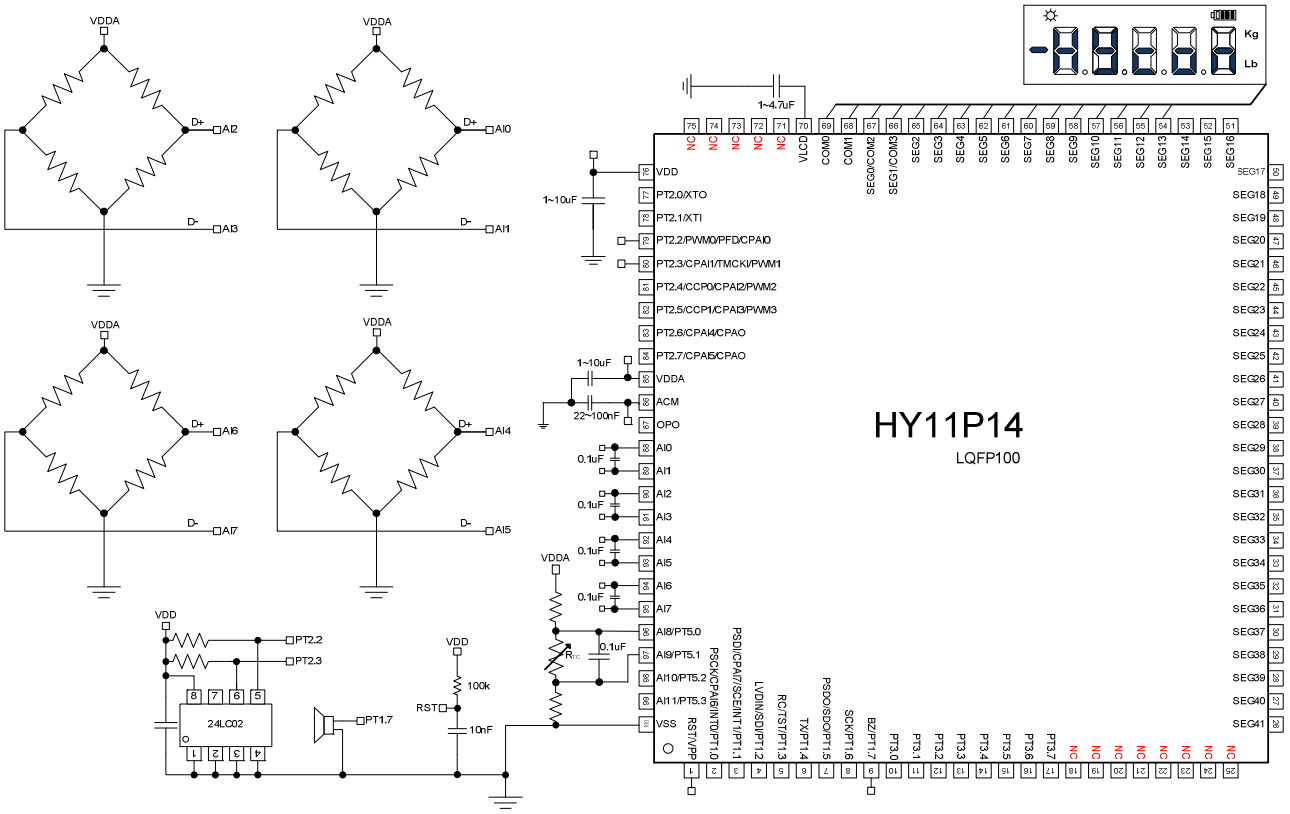


圖 3-1 具溫度補償的橋式感測器應用電路

註：使用溫度補償電阻NTC基本線路

註：關於Load Cell零點電壓位置可透過DCSET[2:0]進行偏壓調整

4. 功能概述

4.1 內部方塊圖

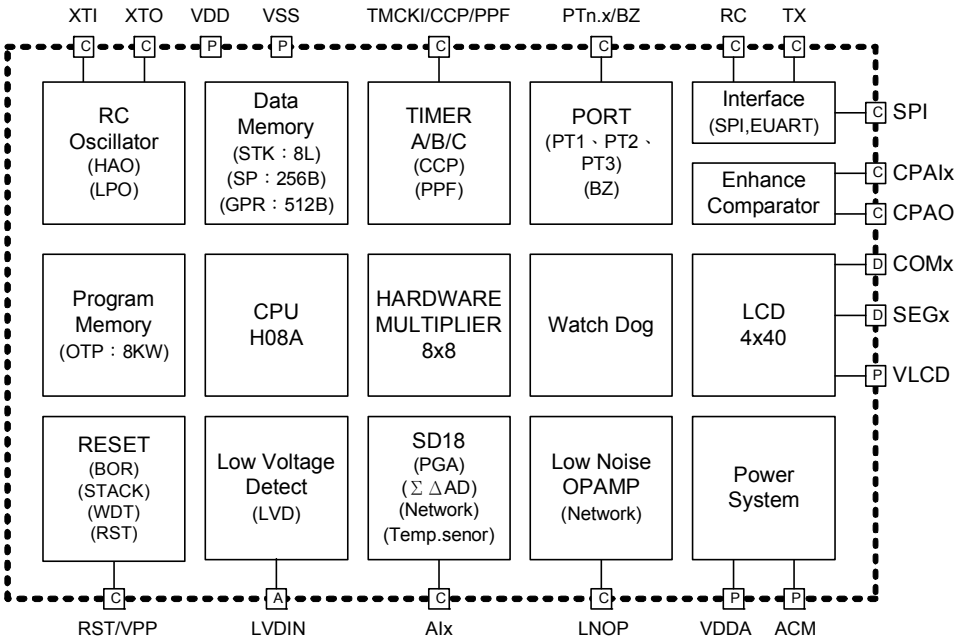


圖 4-1 HY11P14 內部方塊圖

4.2 相關說明與支援文件

晶片功能相關使用說明書

DS-HY11P14-Vxx	HY11P14 說明書
UG-HY11S14-Vxx	HY11Pxx系列使用說明書
APD-CORE002-Vxx	H08A指令說明書

開發工具相關使用說明書

APD-HYIDE006-Vxx	HY11xxx系列開發工具軟體使用說明書
APD-HYIDE005-Vxx	HY11xxx系列開發工具硬體使用說明書
APD-OTP001-Vxx	OTP產品燒錄引腳說明書

產品生產相關使用說明書

APD-HYIDE004-Vxx	HY1xxxx系列生產線專用燒錄器說明書
BDI-HY11P14-Vxx	HY11P14 個別產品的裸片打線資訊

4.3 SD18 Network

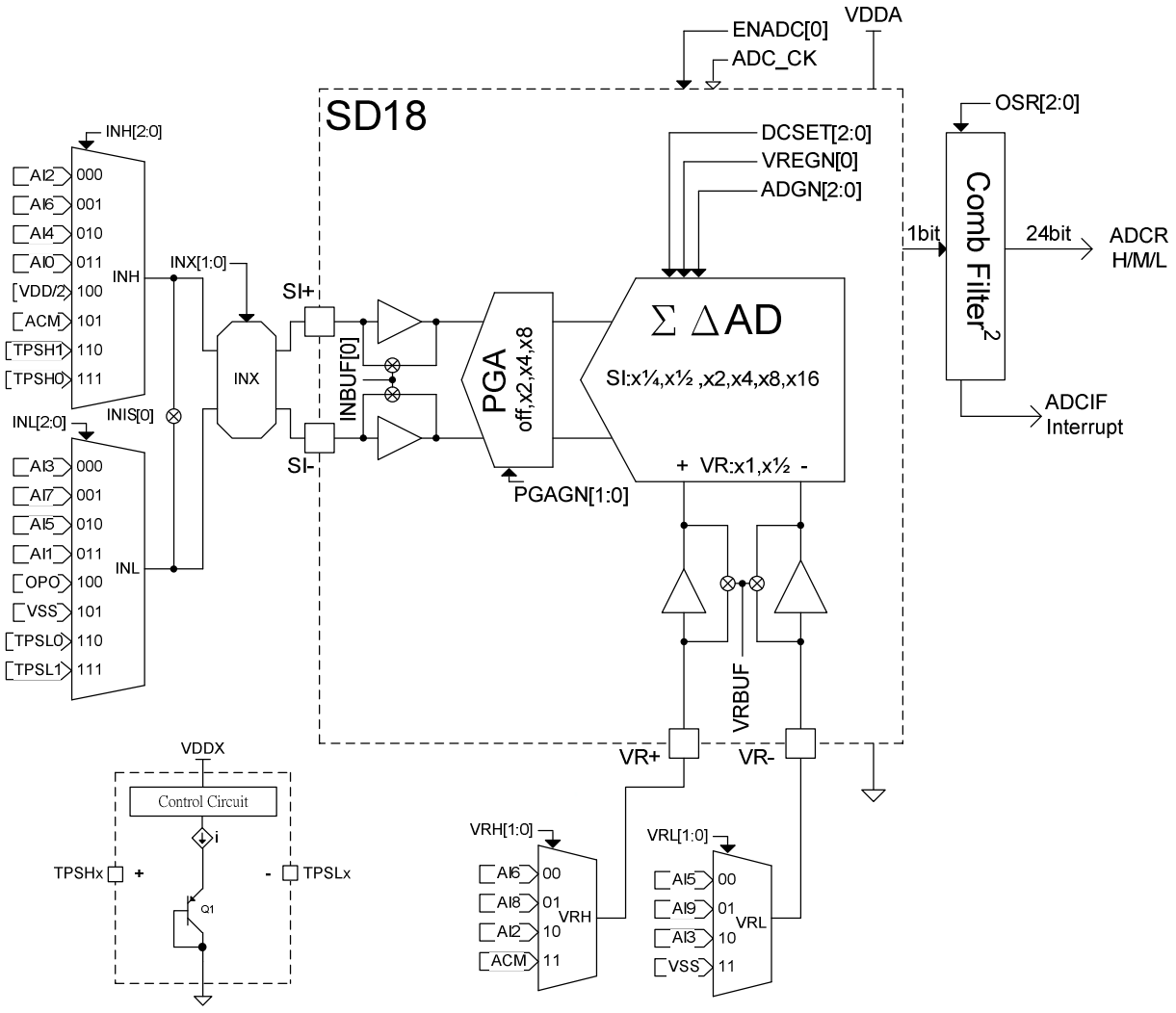


圖 4-2 SD18 Network

4.4 Low Noise OPAMP Network

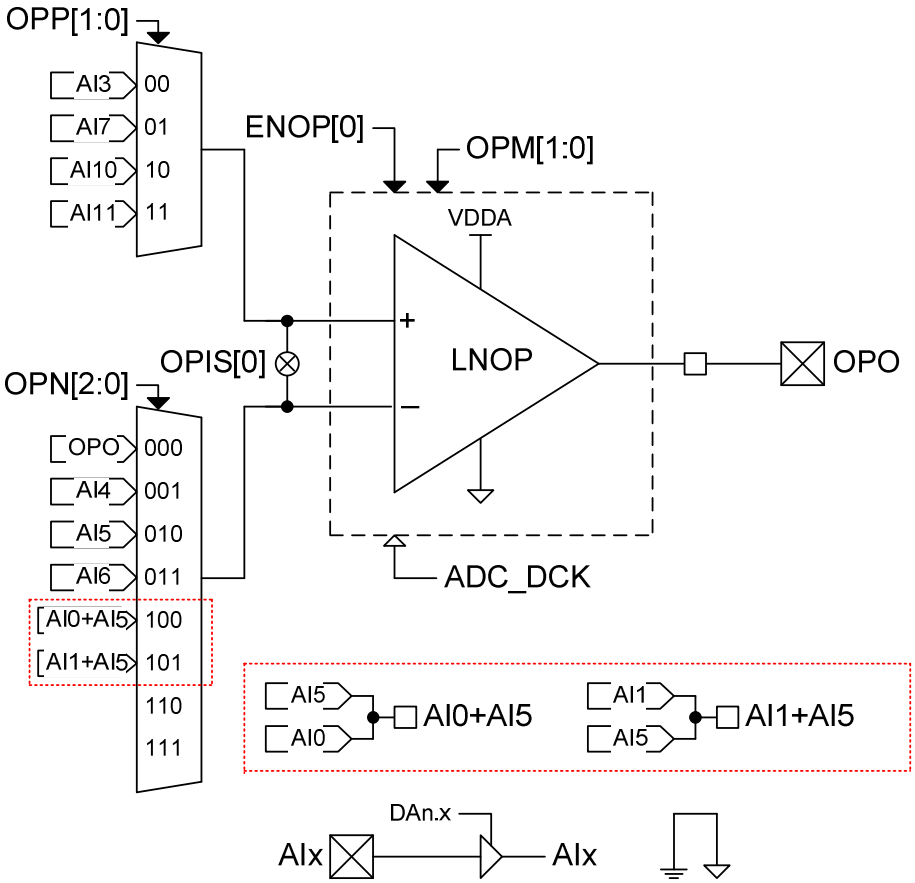


圖 4-3 Low Noise OPAMP Network

4.5 Enhance Comparator Network

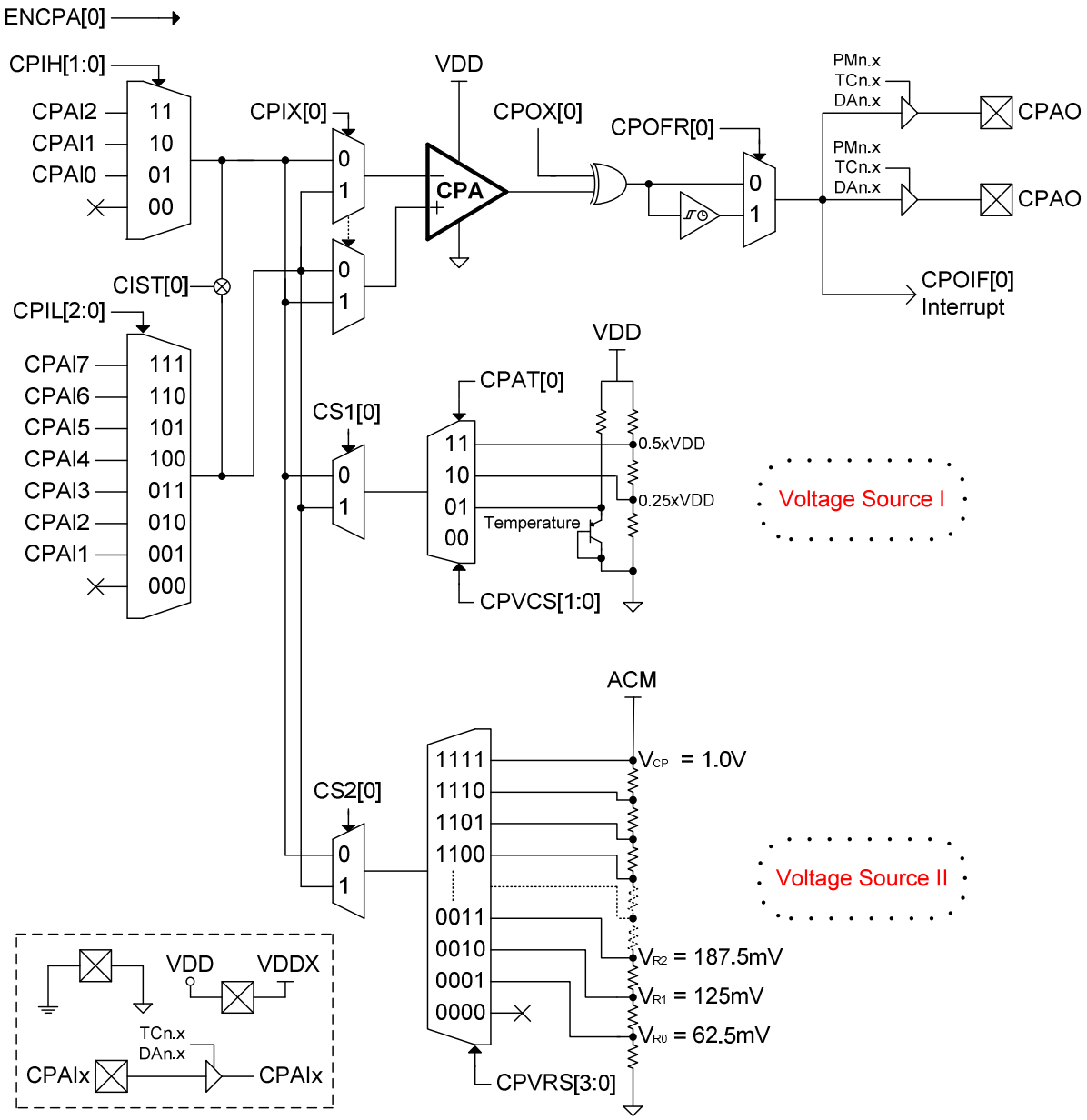


圖 4-4 Enhance Comparator Network

5. 暫存器列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1												
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition												
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**i-RESET**	**R/W**
00H	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
01H	POINC0	Contents of FSR0 to address data memory value of FSR0 post-incremented								N/A	N/A	*,*,*,*,*,*,*,*
02H	PODEC0	Contents of FSR0 to address data memory value of FSR0 post-decremented								N/A	N/A	*,*,*,*,*,*,*,*
03H	PRINC0	Contents of FSR0 to address data memory value of FSR0 pre-incremented								N/A	N/A	*,*,*,*,*,*,*,*
04H	PLUSW0	Contents of FSR0 to address data memory value of FSR0 offset by W								N/A	N/A	*,*,*,*,*,*,*,*
05H	INDF1	Contents of FSR1 to address data memory value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
06H	POINC1	Contents of FSR1 to address data memory value of FSR0 post-incremented								N/A	N/A	*,*,*,*,*,*,*,*
07H	PODEC1	Contents of FSR1 to address data memory value of FSR0 post-decremented								N/A	N/A	*,*,*,*,*,*,*,*
08H	PRINC1	Contents of FSR1 to address data memory value of FSR0 pre-incremented								N/A	N/A	*,*,*,*,*,*,*,*
09H	PLUSW1	Contents of FSR1 to address data memory value of FSR0 offset by W								N/A	N/A	*,*,*,*,*,*,*,*
0FH	FSR0H							FSR0[9]	FSR0[8]	xx	.... ..uu	-,-,-,- -,-,*,*
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
11H	FSR1H							FSR1[9]	FSR1[8]	xx	.... ..uu	-,-,-,- -,-,*,*
12H	FSR1L	Indirect Data Memory Address Pointer 1 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
16H	TOSH				TOS[12]	TOS[11]	TOS[10]	TOS[9]	TOS[8]	...0 0000	...0 0000	-,-,-,*,*,*,*,*
17H	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								0000 0000	0000 0000	*,*,*,*,*,*,*,*
18H	STKPTR	STKFL	STKUN	STKOV		STKPRT[3:0]				000. 0000	000. 0000	r,rw0,rw0,- r,r,r,r
1AH	PCLATH				PC[12]	PC[11]	PC[10]	PC[9]	PC[8]	...0 0000	...0 0000	-,-,-,*,*,*,*,*
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1DH	TBLPTRH				TBLPTR[12]	TBLPTR[11]	TBLPTR[10]	TBLPTR[9]	TBLPTR[8]	...0 0000	...0 0000	-,-,-,*,*,*,*,*
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1FH	TBLDH	Program Memory Table Latch High Byte								0000 0000	0000 0000	*,*,*,*,*,*,*,*
20H	TBLDL	Program Memory Table Latch Low Byte								0000 0000	0000 0000	*,*,*,*,*,*,*,*
21H	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
22H	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
23H	INTE1	GIE	ADCIE	TMCIE	TMBIE	TMAIE	WDTIE	E1IE	E0IE	0000 0000	0000 0000	*,*,*,*,*,*,*,*
24H	INTE2	TXIE	RCIE			CPOIE	SSPIE	CCP1IE	CCP0IE	00.. 0000	00.. 0000	*,*,-,-,*,*,*,*
26H	INTF1		ADCIF	TMCIF	TMBIF	TMAIF	WDTIF	E1IF	E0IF	.000 0000	.000 0000	-,*,*,*,*,*,*,*
27H	INTF2	TXIF	RCIF			CPOIF	SSPIF	CCP1IF	CCP0IF	00.. 0000	00.. 0000	*,*,-,-,*,*,*,*
29H	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
2AH	BSRCN							BSR[1]	BSR[0]	00	00	-,-,-,- -,-,*,*
2BH	STATUS				C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
2CH	PSTATUS	PD	TO	IDLEB	BOR		SKERR			000d .0..	uduu .d..	rw0,rw0,rw0,rw0 -,rw0,-,-
2DH	LVDCN		LVDFG	LVD	LVDON	VLDX[3:0]				.000 0000	.000 uuuu	-,*,r,r,*,*,*,*
30H	PWRCN	ENVDDA	VDDAX[1:0]		ENACM					0000	0000	*,*,*,*,-,-,-,-
31H	MCKCN1	ADCS[2:0]			ADCCK	XTHSP	XTSP	ENXT	ENHAO	0000 0001	0000 0001	*,*,*,*,*,*,*,*
32H	MCKCN2			LSCK	HSCK	HSS[1:0]		CPUCK[1:0]		..00 0000	..00 0000	-,-,*,*,*,*,*,*
33H	MCKCN3	LCDS[2:0]				PERCK	BZS[2:0]			000. 0000	000. 0000	*,*,*,-,*,*,*,*
34H	CPACN1	ENCPA	CPIST	CPIX	CPIH[1:0]		CPIL[2:0]			0000 0000	0000 0000	*,*,*,*,*,*,*,*
35H	CPACN2		CPOX	CPOFR	CS1	CPAT	CPVCS[1:0]			.000 000.	.000 000.	-,*,*,* r,*,*,*
36H	CPACN3				CS2	CPVRX[3:0]				...0 0000	...0 0000	-,-,-,*,*,*,*,*
37H	OPCN1	ENOP	OPM[1:0]		OPP[1:0]		OPN[2:0]			0000 0000	0000 0000	*,*,*,*,*,*,*,*
39H	ADCRH	ADC conversion memory HighByte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3AH	ADCRM	ADC conversion memory Middle Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3BH	ADCRL	ADC conversion memory Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3CH	ADCCN1	ENADC	ENHIGN	ENCHP	PGAGN[1:0]		ADGN[2:0]			0000 0000	0000 0000	*,*,*,*,*,*,*,*
3DH	ADCCN2			INBUF	VRBUF	VREGN	DCSET[2:0]			..00 0000	..00 0000	-,-,*,*,*,*,*,*
3EH	ADCCN3	OSR[2:0]								000.	000.	*,*,*,-,-,-,-,-
3FH	AINET1	INH[2:0]			INL[2:0]			INIS	OPIS	0000 0000	0000 0000	*,*,*,*,*,*,*,*
40H	AINET2		VRH[1:0]		INX[1:0]		VRL[1:0]			.000 000.	.000 000.	-,*,*,*,*,*,*,-
41H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDTS[2:0]			0000 0000	0000 0000	*,*,*,* w1,*,*,*
42H	TMAR	TimerA data register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
43H	TMBCN	ENTMB	TMBCK	TMBS[1:0]		TMBSYC	TMBR2R			0000 00..	0000 00..	*,*,*,*,*,*,-,-
44H	TMBRH	TimerB High Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
45H	TMBRL	TimerB Low Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
46H	TMCCN	ENTMC	TMCCK[1:0]		TMCS1[2:0]			TMCS0[1:0]		0000 0000	0000 0000	*,*,*,*,*,*,*,*
47H	PRC	TimerC programmable register								1111 1111	1111 1111	*,*,*,*,*,*,*,*
48H	TMCR	TimerC register								0000 0000	0000 0000	r,r,r,r r,r,r,r
49H	CCPCN	CCP1M[3:0]				CCP0M[3:0]				0000 0000	0000 0000	*,*,*,*,*,*,*,*
4AH	CCP0RH	CCP0 High Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
4BH	CCP0RL	CCP0 Low Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
4CH	CCP1RH	CCP1 High Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
4DH	CCP1RL	CCP1 Low Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
4EH	PASC	PASF		PASCF[1:0]		PSSCN0[1:0]		PSSCN1[1:0]		0.00 0000	0.00 0000	*,-,*,*,*,*,*,*
4FH	PWMCN	ENPWM	ENPFD	PWMRL[1:0]		PWMCG[1:0]		PWMM[1:0]		0000 0000	0000 0000	*,*,*,*,*,*,*,*
50H	PDBD	ENPRS	DBDC[6:0]							0000 0000	0000 0000	*,*,*,*,*,*,*,*
51H	PWMR	PWM MSB Byte register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-1(a) HY11P14 暫存器列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1												
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition												
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**i-RESET**	**R/W**
52H	LCDCN1	ENLCD	LCDPR	VLCDX[1:0]		LCDBF	LCDBI[1:0]			0000 000.	0000 000.	*,*,*,*,*,*,-
53H	LCDCN2	LCDBL	LCDMX[1:0]							000.	000.	*,*,*,-,-,-,-
54H	LCD0	Segment SEG2@[3:0] and SEG3@[7:4] data register of LCD0								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
55H	LCD1	Segment SEG4@[3:0] and SEG5@[7:4] data register of LCD1								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
56H	LCD2	Segment SEG6@[3:0] and SEG7@[7:4] data register of LCD2								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
57H	LCD3	Segment SEG8@[3:0] and SEG9@[7:4] data register of LCD3								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
58H	LCD4	Segment SEG10@[3:0] and SEG11@[7:4] data register of LCD4								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
59H	LCD5	Segment SEG12@[3:0] and SEG13@[7:4] data register of LCD5								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
5AH	LCD6	Segment SEG14@[3:0] and SEG15@[7:4] data register of LCD6								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
5BH	LCD7	Segment SEG16@[3:0] and SEG17@[7:4] data register of LCD7								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
5CH	LCD8	Segment SEG18@[3:0] and SEG19@[7:4] data register of LCD8								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
5DH	LCD9	Segment SEG20@[3:0] and SEG21@[7:4] data register of LCD9								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
5EH	SSPCON1	SSPEN	CKP	CKE	SMP	–	–	SSPM<1:0>		0000 ..00	uuuu ..uu	*,*,*,-,-,*,*
60H	SSPSTA	SSPBUY	SSPOV	Reserve for IIC					BF	00.. ...0	00.. ...0	r,r,-,- -,-,-,r
61H	SSPBUF	SSP Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
63H	URCON	ENSP	ENTX	TX9	TX9D	PARITY			WUE	0000 0..0	0000 0..0	*,*,*,*,-,-,*
64H	URSTA		RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0110	.000 0110	-,r,r,r r r,r,r,rw0
65H	BAUDCON					ENCR	RC9	ENADD	ENABD	 0000	 0000	-,-,-,- *,*,*,*
66H	BRGRH				Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,*,*,*,*
67H	BRGRL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
68H	TXREG	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
69H	RCREG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
6DH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	*,*,*,* r,r,r,r
6EH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4					0000	0000	*,*,*,*,-,-,-,-
6FH	PT1DA						DA1.2	DA1.1	DA1.0	.... .000	.... .000	-,-,-,- -,*,*,*
70H	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
71H	PT1M1					INTEG1[1:0]		INTEG0[1:0]		 0000	 0000	-,-,-,- *,*,*,*
72H	PT1M2		PM1.7[0]		PM1.6[0]		PM1.5[0]		PM1.4[0]	.0.0 .0.0	.0.0 .0.0	-,*,-,*,-,*,-,*
74H	PT2	PT2.7	PT2.6	PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
75H	TRISC2	TC2.7	TC2.6	TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
76H	PT2DA	DA2.7	DA2.6	DA2.5	DA2.4	DA2.3	DA2.2			0000 00..	0000 00..	*,*,*,*,*,-,-
77H	PT2PU	PU2.7	PU2.6	PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
78H	PT2M1		PM2.3[0]	PM2.2[1]	PM2.2[0]					.000	.000	-,*,*,* -,-,-,-
79H	PT2M2	PWMTR[1:0]			PM2.6[0]	PM2.5[1]	PM2.5[0]	PM2.4[1]	PM2.4[0]	00.0 0000	00.0 0000	*,*,-,*,*,*,*,*
7AH	PT3	PT3.7	PT3.6	PT3.5	PT3.4	PT3.3	PT3.2	PT3.1	PT3.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
7BH	TRISC3	TC3.7	TC3.6	TC3.5	TC3.4	TC3.3	TC3.2	TC3.1	TC3.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
7DH	PT3PU	PU3.7	PU3.6	PU3.5	PU3.4	PU3.3	PU3.2	PU3.1	PU3.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
80H ~ FFH		GENERAL PURPOSE REGISTER @ 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
100H~17FH		GENERAL PURPOSE REGISTER @ 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
180H	LCD10	Segment SEG22@[3:0] and SEG23@[7:4] data register of LCD10								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
181H	LCD11	Segment SEG24@[3:0] and SEG25@[7:4] data register of LCD11								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
182H	LCD12	Segment SEG26@[3:0] and SEG27@[7:4] data register of LCD12								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
183H	LCD13	Segment SEG28@[3:0] and SEG29@[7:4] data register of LCD13								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
184H	LCD14	Segment SEG30@[3:0] and SEG31@[7:4] data register of LCD14								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
185H	LCD15	Segment SEG32@[3:0] and SEG33@[7:4] data register of LCD15								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
186H	LCD16	Segment SEG34@[3:0] and SEG35@[7:4] data register of LCD16								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
187H	LCD17	Segment SEG36@[3:0] and SEG37@[7:4] data register of LCD17								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
188H	LCD18	Segment SEG38@[3:0] and SEG39@[7:4] data register of LCD18								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
189H	LCD19	Segment SEG40@[3:0] and SEG41@[7:4] data register of LCD19								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
192H	PT5					PT5.3	PT5.2	PT5.1	PT5.0	 xxxx	.... uuuu	-,-,-,- r,r,r,r
193H	PT5DA					DA5.3	DA5.2	DA5.1	DA5.0	 1111	 1111	-,-,-,- *,*,*,*
194H	PT5PU					PU5.3	PU5.2	PU5.1	PU5.0	 0000	 0000	'-,-,-,- *,*,*,*
200H ~ 2FFH		GENERAL PURPOSE REGISTER @ 256Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

圖 5-1(b) HY11P14 暫存器列表(續)

6. 電氣特性

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . . −0.2 V to 4.0 V

Voltage applied to any pin . . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . . −0.2 V to 6.9 V

Voltage applied to TST/PT1.3 pin . . . . . −0.2 V to V_{DD} + 1 V

Diode current at any device terminal . . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . . −55℃ to 150℃

(programmed device) . . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any PORT1 to PORT3 I/O pin. 25mA

6.1 Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage		All digital peripherals and CPU		2.2		3.6	V
			Analog peripherals		2.4		3.6	
V_{SS}	Supply Voltage				0		0	
XT	External Oscillator Frequency	Watch crystal	V_{DD} = 2.2V, ENXT[0]=1	XTSP[0]=0, XTHSP[0]=0	32.768K			Hz
		Ceramic resonator		XTSP[0]=1, XTHSP[0]=0	450K		8M	
		Crystal		XTSP[0]=1, XTHSP[0]=0	1M		8M	

6.2 Internal RC Oscillator

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.8	2.0	2.2	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	22	28	35	KHz

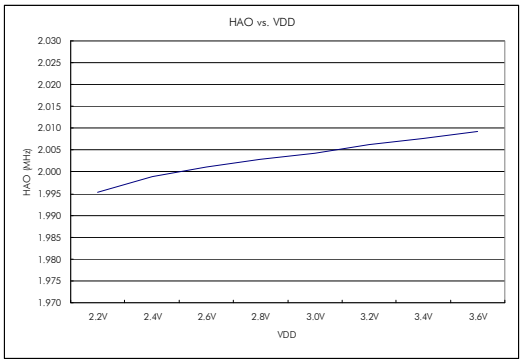


Figure 6.2-1 HAO vs. VDD

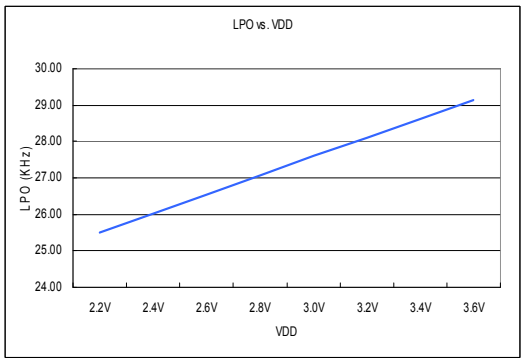


Figure 6.2-2 LPO vs. VDD

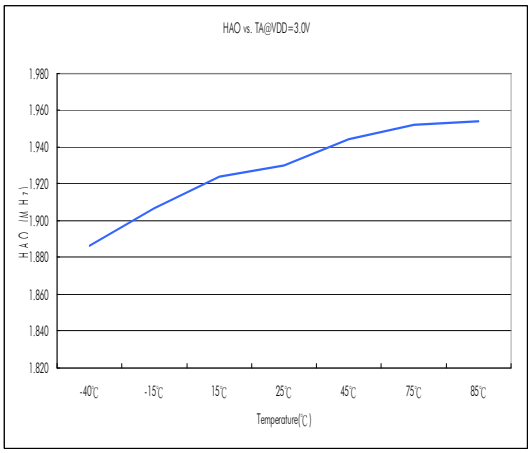


Figure 6.2-3 HAO vs. Temperature

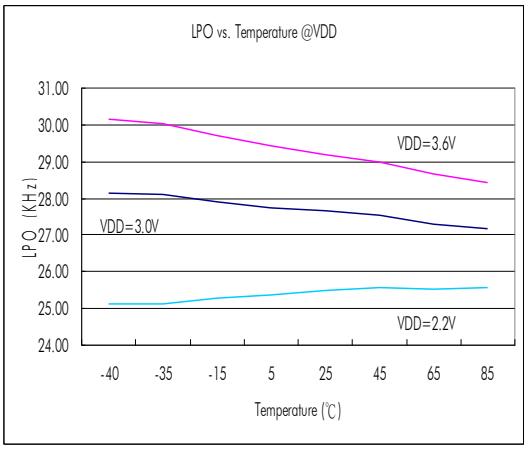


Figure 6.2-4 LPO vs. Temperature

6.3 Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 28KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = 8MHz, OSC_HAO = off, CPU_CK = 8MHz		1.34	2	mA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.36	0.55	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.2	0.3	mA
I_{LP1}	Low Power 1	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 16384Hz		7	12	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_CY：External Oscillator frequency.

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

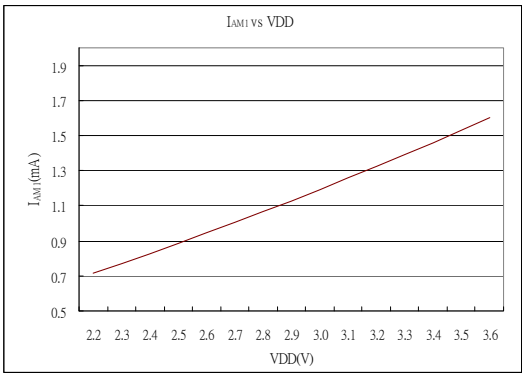


Figure 6.3-1 I_{AM1} vs. VDD

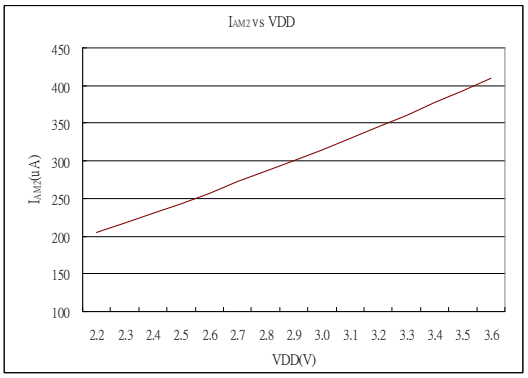


Figure 6.3-2 I_{AM2} vs. VDD

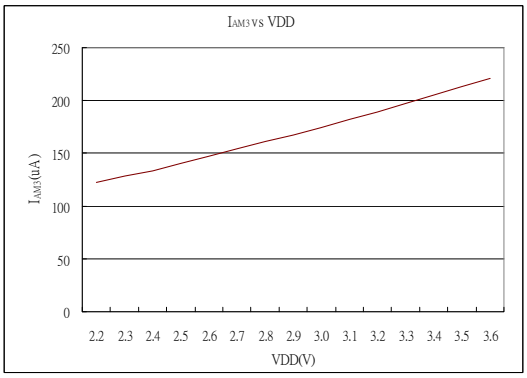


Figure 6.3-3 I_{AM3} vs. VDD

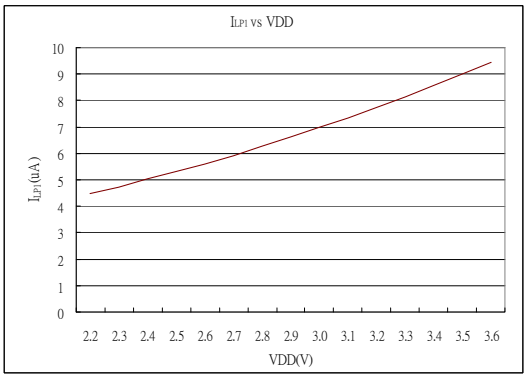


Figure 6.3-4 I_{LP1} vs. VDD

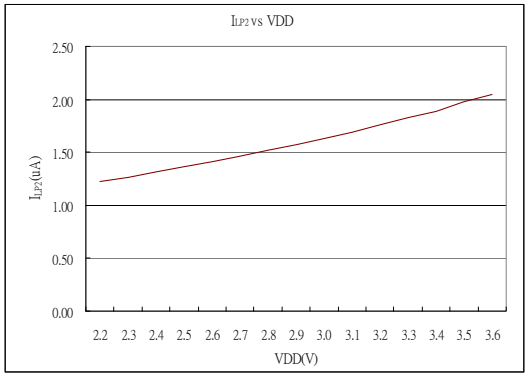


Figure 6.3-5 I_{LP2} vs. VDD

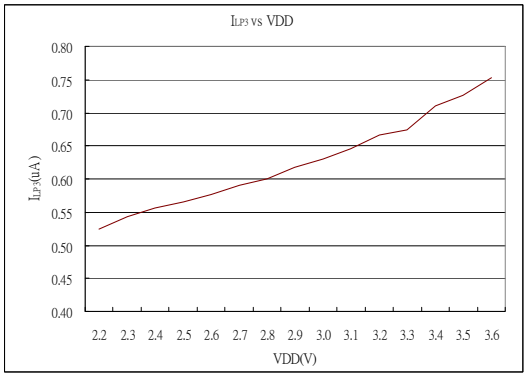


Figure 6.3-6 I_{LP3} vs. VDD

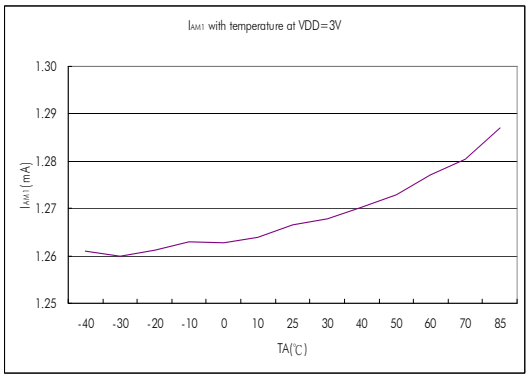


Figure 6.3-7 I_{AM1} vs. Temperature

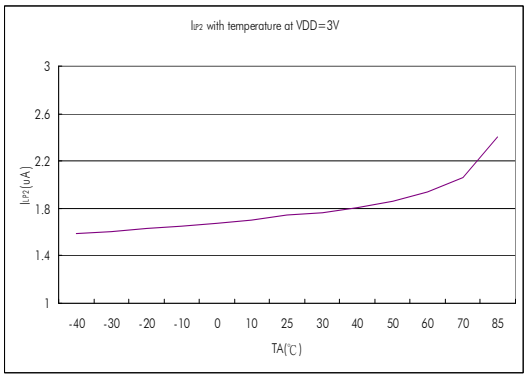


Figure 6.3-8 I_{LP2} vs. Temperature

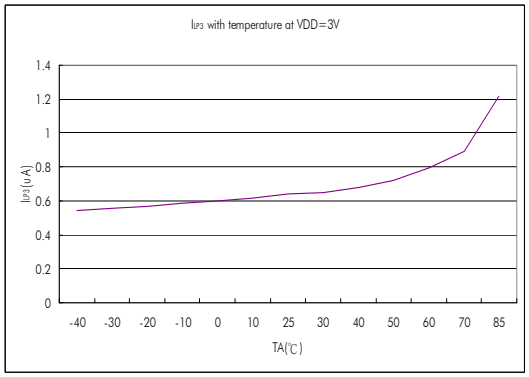


Figure 6.3-9 I_{LP3} vs. Temperature

6.4 Port1~5

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			180		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	I_{OH}=10mA	V_{DD} -0.3			V
V_{OL}	Low-level output voltage	I_{OL}=-10mA			VSS +0.3	

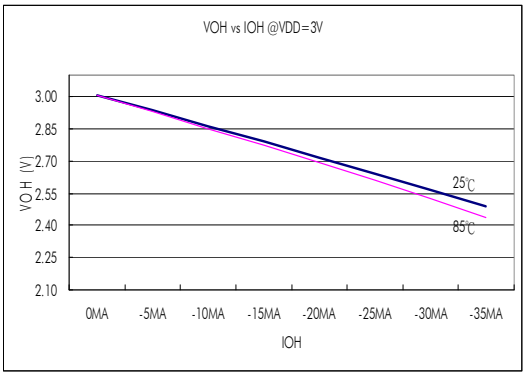


Figure 6.4-1 V_{OH} vs. I_{OH} @VDD=3.0V

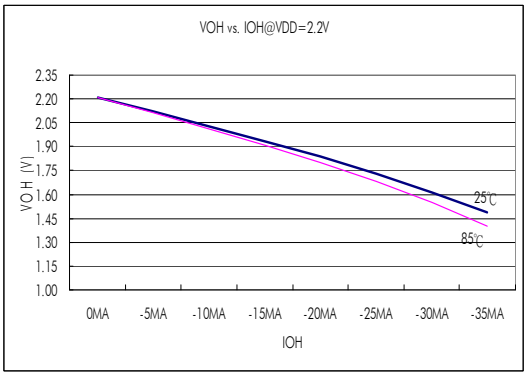


Figure 6.4-2 V_{OH} vs. I_{OH} @VDD=2.2V

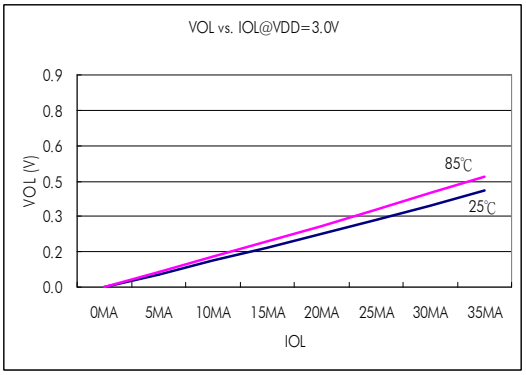


Figure 6.4-3 V_{OL} vs. I_{OL}@VDD=3.0V

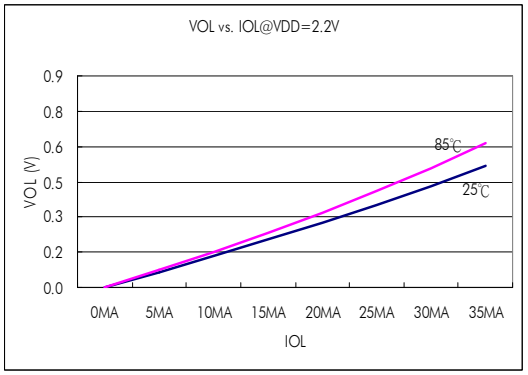


Figure 6.4-4 V_{OL} vs. I_{OL}@VDD=2.2V

6.5 Reset(Brownout, External RST pin, Low Voltage Detect)

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS-LVR}$			70		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS-RST}$			0.8		V
LVD	Operation current, I_{LVD}			10	15	uA
	External input voltage to compare reference voltage			1.2		V
	Compare reference voltage temperature drift	T_A = -40℃ ~ 85 ℃		100		ppm/℃
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1110b			3.3		V
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1101b			3.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1100b			3.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1011b			3.0		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1010b			2.9		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1001b			2.8		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1000b			2.7		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0111b			2.6		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0110b			2.5		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0101b			2.4		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0100b			2.3		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0011b			2.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0010b			2.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0001b			2.0		

BOR：Brownout Reset

LVR：Low Voltage Reset of BOR

LVD：Low Voltage Detect

RST：External Reset pin

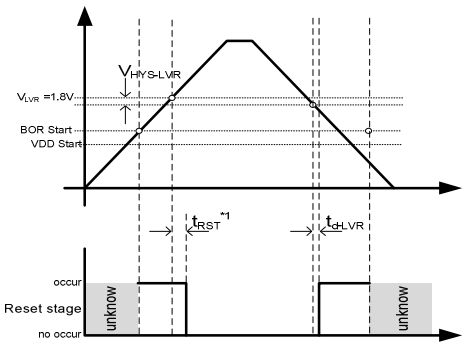


Figure6.5-1 BOR reset diagram

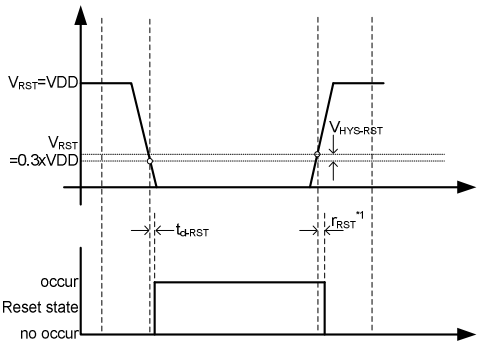


Figure6.5-2 RST reset diagram

*1 r_{RST}：Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).

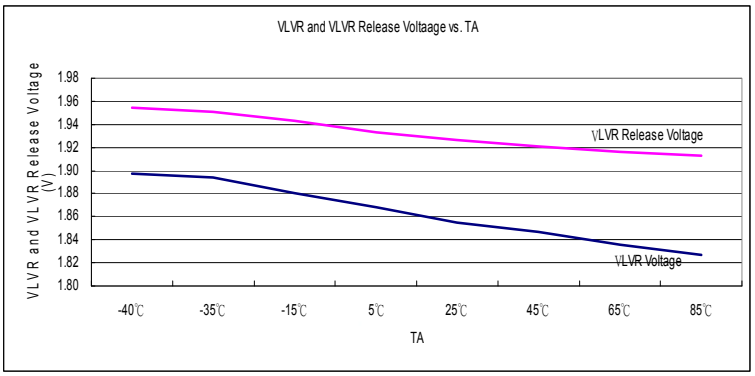


Figure6.5-3 LVR vs. Temperature

6.6 Power System

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	VDDAX[1:0]=00b		22		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.2V	VDDAX[1:0]=00b		3.3		V
			VDDAX[1:0]=01b		2.9		V
			VDDAX[1:0]=10b		2.6		V
			VDDAX[1:0]=11b		2.4		V
	Dropout voltage	I_L = 10mA	VDDAX[1:0]=00b		135		mV
			VDDAX[1:0]=01b		150		mV
			VDDAX[1:0]=10b		165		mV
			VDDAX[1:0]=11b		180		mV
	Temperature drift	VDDAX[1:0]=11b	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift	I_L = 0.1mA	V_{DD}=2.5V~3.6V		±0.2		%/V
ACM	ACM operation current, I_{ACM}	I_L = 0mA			20		uA
	Output voltage ,V_{ACM}	ENACM[0]=1, *1	I_L = 0uA		1.0		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Output voltage ,V_{ACM}	ENACM[0]=1, *2	I_L = 0uA		1.2		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Temperature drift	ENACM[0]=1,	T_A=-40℃~85℃		50		ppm/℃
	VDDA Voltage drift	I_L = 10uA			100		uV/V

VDDA：Adjust Voltage Regulator

ACM：Analog Common Mode Voltage

*1: V_{ACM} = 1.0V is just for VDDAX[1:0]=1xb mode. (at A/D differential voltage reference < 1.4V)

*2: V_{ACM} = 1.2V is just for VDDAX[1:0]=0xb mode. (at A/D differential voltage reference > 1.4V)

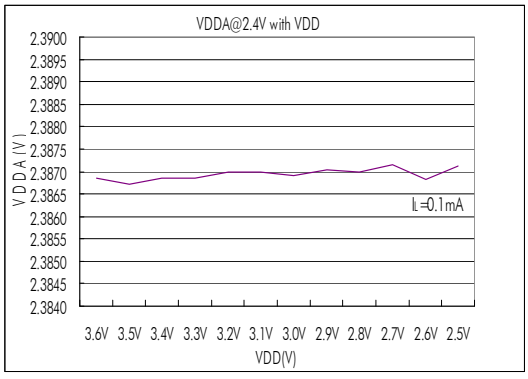


Figure6.6-1 VDDA I_L=0.1mA vs. VDD

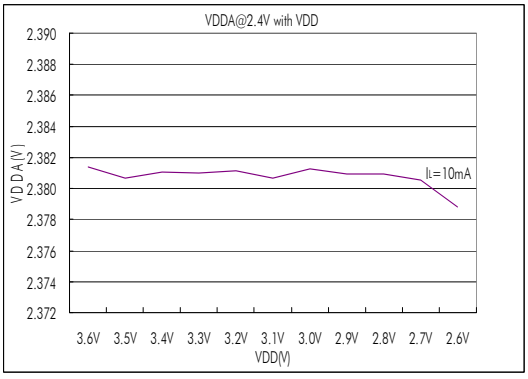


Figure6.6-2 VDDA I_L=10mA vs. VDD

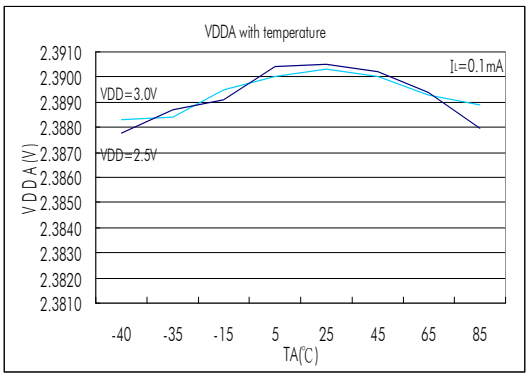


Figure6.6-3 VDDA I_L=0.1mA vs. Temperature

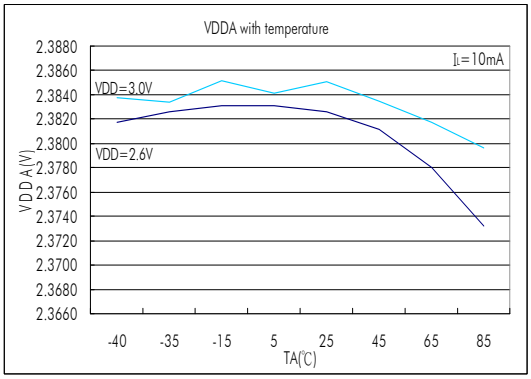


Figure6.6-4 VDDA I_L=10mA vs. Temperature

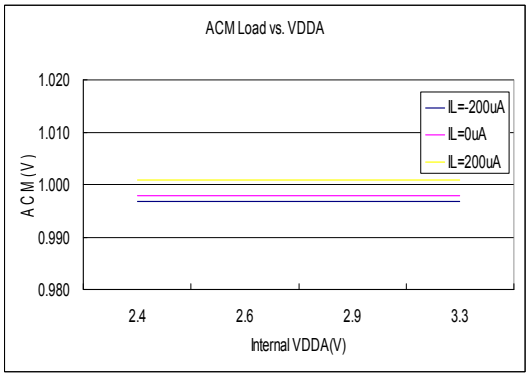


Figure6.6-5 ACM Load vs. VDDA (a)

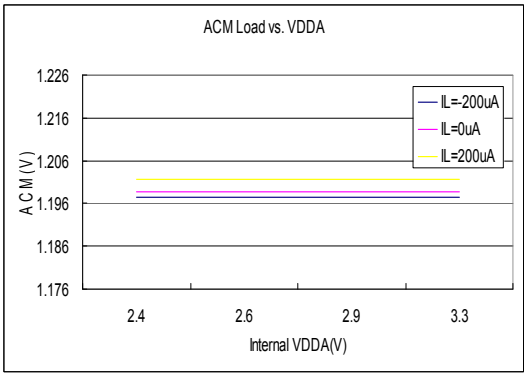


Figure6.6-5 ACM Load vs. VDDA (b)

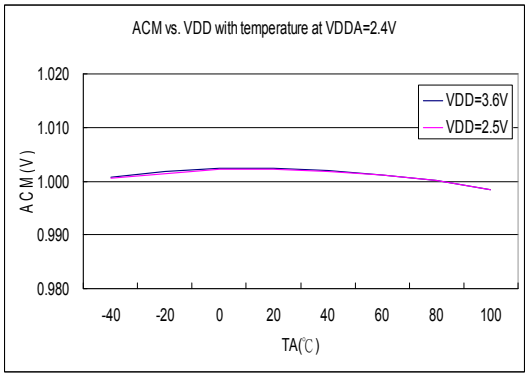


Figure6.6-6 ACM vs. Temperature (a)

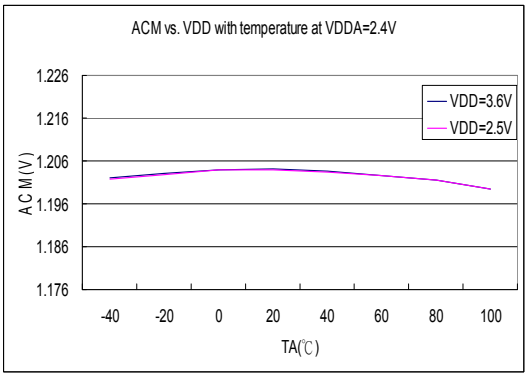


Figure6.6-6 ACM vs. Temperature (b)

6.7 LCD

T_A = 25℃,V_{DD} = 3.0V, C_{VLCD} =4.7uF,unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.(all segment turn on)	LCDPR[0]=1 LCDS_CK=122hz	V_{DD} = 2.2V		10		uA
			V_{DD} = 3.0V				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2		3.6	V
	Embedded Charge Pump output voltage at VLCD pin	V_{DD} = 2.2V, LCDPR[0]=1, C_{VLCD} =4.7uF	VLCDX[1:0]=11b	2.295	2.55	2.805	V
			VLCDX[1:0]=10b	2.52	2.8	3.08	
			VLCDX[1:0]=01b	2.745	3.05	3.355	
			VLCDX[1:0]=00b	2.97	3.3	3.63	
Z_{LCD}	Output impedance with LCD buffer	f_{LCD} =128Hz,VLCD=3.05V			10		kΩ

曲線圖：

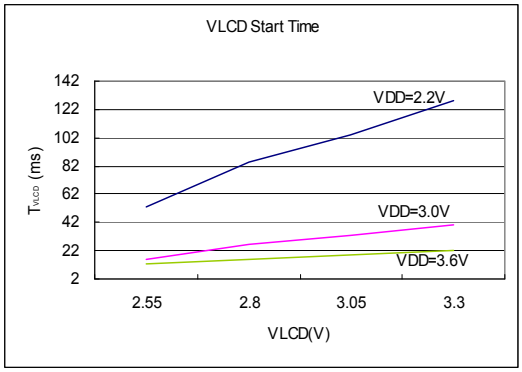


Figure6.7-1 LCD start time

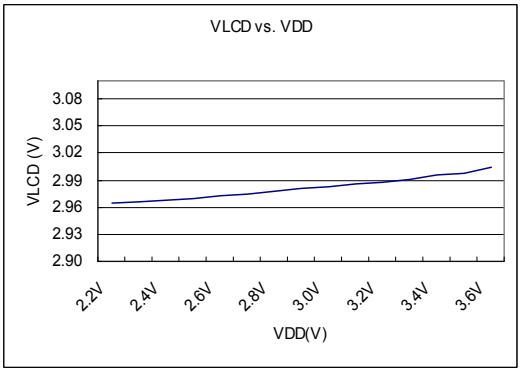


Figure6.7-2 VLCD vs. VDD

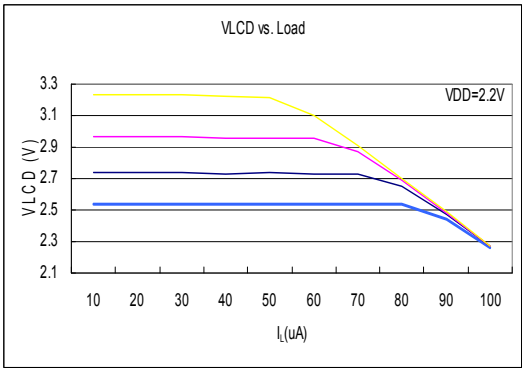


Figure6.7-3 VLCD vs. I_L @VDD=2.2V

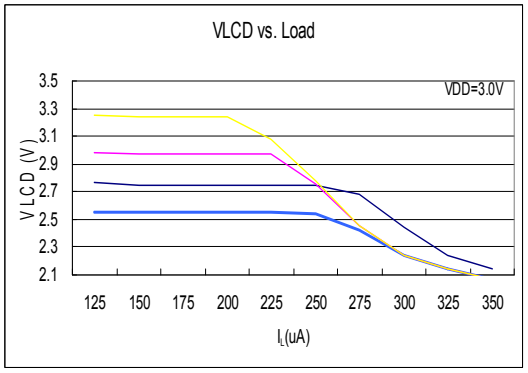


Figure6.7-4 VLCD vs. I_L @VDD=3.0V

6.8 Low Noise OPAMP

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{LNOP}	Supply voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{LNOP}	Operation supply current		OPM[1:0]=xxb		200		uA
V_{OS-OP}	Input offset voltage without chopper.		OPM[1:0]=1xb	-2		2	mV
	Input offset voltage with chopper		OPM[1:0]=0xb		20		uV
	Input offset voltage temperature drift.	OPM[1:0]=00b	T_A=-40℃~85℃		0.1		uV/℃
		OPM[1:0]=10			2		
V_{OLR}	Unit gain load regulation	V_O=1.2V, VDDA=2.4V	I_L=+1mA		0.1		%V_O
			I_L=-1mA				
CMVR	Common-mode voltage input range		OPM[1:0]=xxb	0.1		VDDA-1.1	V
CMRR	Common-mode rejection ratio		OPM[1:0]=xxb		90		dB

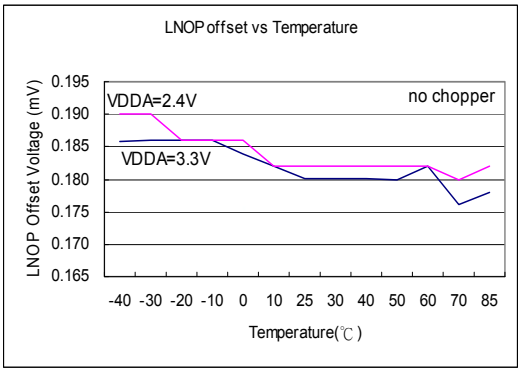


Figure6.8-1 LNOP Offset Temperature

6.9 SD18,Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			256		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1 INBUF[0]=1,VRBUF[0]=0	GAIN =4, ADC_CK=250KHz		168		uA
		ENADC[0]=1 INBUF[0]=0,VRBUF[0]=1			150		
		ENADC[0]=1 INBUF[0]=0,VRBUF[0]=0			120		

6.10 PGA,Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<01>or<1x>			320		uA
G_{PGA}	Gain temperature drift	T_A = -40℃~ 85℃	GAIN=128		5		ppm/℃

6.11 SD18,performance Ⅱ (fSD18=250KHz)

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.9V,V_{VR}=1.0V,GAIN=1 without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}=1.0V,ΔSI=±200mV			±0.003	±0.01	%FSR
		VDDA=2.4V,V_{VR}=1.0V,ΔSI=±450mV					
	No Missing Codes[3]	ADC_CK=250KHz,OSR[2:0]=010b		23			Bits
G_{SD18}	Temperature drift Gain 1~x16 (INBUF[0]=0b) Gain 1~x4 (INBUF[0]=1b)	INBUF[0]=0b,VRBUF[0]=0b	T_A = -40℃~ 85℃		2		ppm/℃
		INBUF[0]=1b,VRBUF[0]=0b					
		INBUF[0]=0b,VRBUF[0]=1b					
		INBUF[0]=1b,VRBUF[0]=1b					
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper and Buffer(INBUF,VRBUF) without PGA	ΔAI=0V ΔVR=0.9V DCSET[2:0]=<000> *ΔAI is external short	Gain=2			1	%FSR
	Offset error of Full Scale Rang input voltage range with Chopper without PGA and Buffer(INBUF,VRBUF)		Gain=2			1	

	Offset temperature drift with chopper without PGA and Buffer (INBUF,VRBUF).		GAIN=1	2	uV/℃
			GAIN=2	1	
			GAIN=4	0.5	
			GAIN=16	0.15	
	Offset temperature drift with chopper and Buffer (INBUF,VRBUF) without PGA.		GAIN=1	2	
			GAIN=2	1	
			GAIN=4	0.5	
	Offset temperature drift with chopper without Buffer (INBUF,VRBUF).		GAIN=128	0.02	
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,without PGA	V_{SI}=0V, GAIN=1	90	dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V, without PGA	V_{SI}=0V, GAIN=16	75	
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA=±100mV,V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1 PGA=off	75	dB
			GAIN=16 PGA=8		

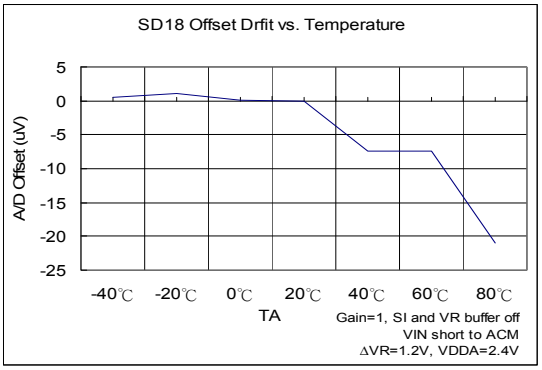


Figure6.9-1(a) SD18 Offset Temperature drift

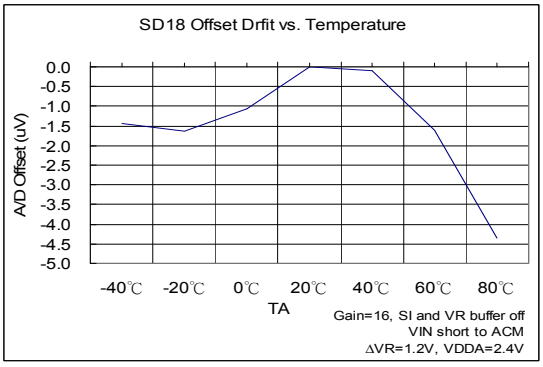


Figure6.9-1(b) SD18 Offset Temperature drift

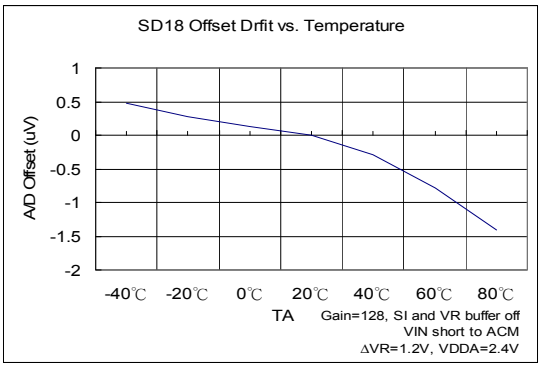


Figure6.9-1(c) SD18 Offset Temperature drift

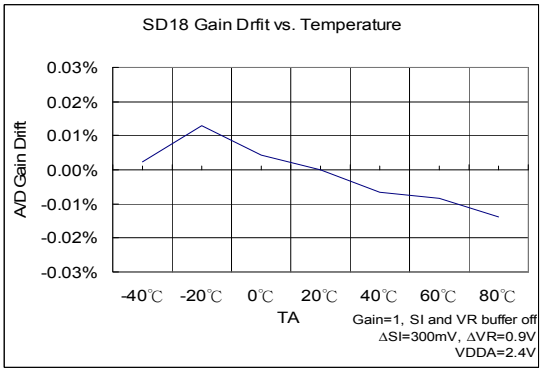


Figure6.9-2(a) SD18 Gain drift with temperature

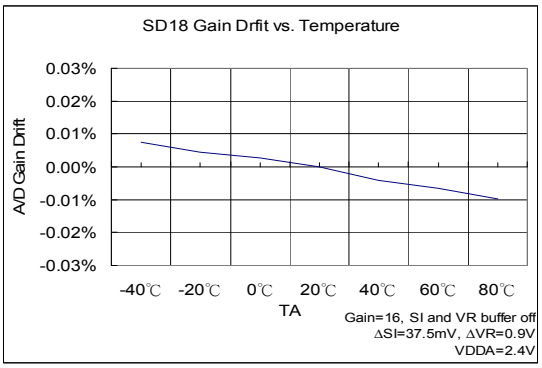


Figure6.9-2(b) SD18 Gain drift with temperature

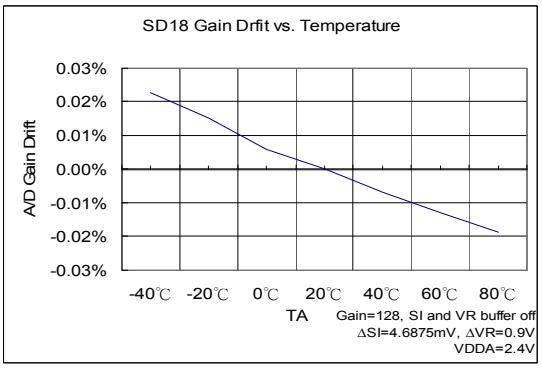


Figure6.9-2(c) SD18 Gain drift with temperature

6.12 SD18,Temperature sensor

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift			178		uV/℃
KT	Absolute Temperature Scale 0°K	INBUF[0]=1		-289		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

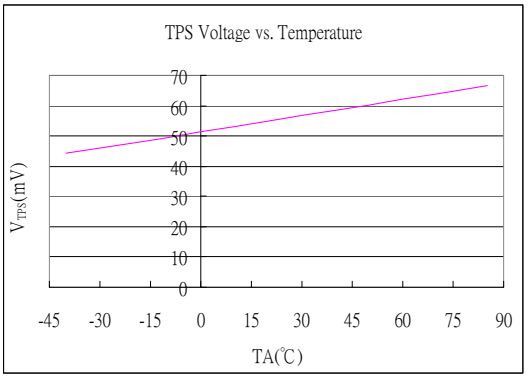


Figure6.9-3 TPS output voltage vs. temperature drift

6.13 SD18 Noise Performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

HY11P14 針對SD18 提供了重要的輸入雜訊規格。Table6.9-4(a), Table6.9-4(b) 列出典型的雜訊規格表與Gain, Output rate, 及單端最大輸入電壓等關係。測試條件設定在外部輸入訊號短路，參考電壓為 1.2V，取樣 1024 筆資料。

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF (1)	OSR					256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN								
±2400	0.25	=	1	×	0.25	16.3	17.4	17.9	18.5	19.0	19.5	20.0	20.4
±2160	0.5	=	1	×	0.5	16.3	17.3	17.9	18.4	18.9	19.4	19.8	20.2
±1080	1	=	1	×	1	16.2	17.2	17.8	18.3	18.8	19.3	19.7	20.1
±540	2	=	1	×	2	16.1	17.1	17.6	18.2	18.7	19.2	19.6	20.0
±270	4	=	1	×	4	16.0	16.9	17.5	18.0	18.5	18.9	19.4	19.8
±135	8	=	1	×	8	15.9	16.6	17.2	17.7	18.2	18.7	19.2	19.6
±68	16	=	1	×	16	15.6	16.3	16.8	17.3	17.7	18.3	18.8	19.3
±34	32	=	2	×	16	14.8	15.3	15.9	16.4	16.9	17.4	17.8	18.3
±17	64	=	4	×	16	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0
±8	128	=	8	×	16	14.0	14.6	15.1	15.6	16.0	16.6	17.0	17.5

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table6.9-4(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF	OSR					256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN								
±2400	0.25	=	1	×	0.25	121.08	57.40	38.74	26.66	18.39	13.21	9.49	6.98
±2160	0.5	=	1	×	0.5	61.63	29.23	19.21	13.51	9.78	7.02	5.12	3.91
±1080	1	=	1	×	1	32.21	15.70	10.25	7.31	5.19	3.77	2.80	2.13
±540	2	=	1	×	2	16.59	8.54	5.91	4.06	2.86	2.06	1.48	1.12
±270	4	=	1	×	4	9.00	4.84	3.33	2.37	1.67	1.19	0.87	0.65
±135	8	=	1	×	8	5.04	2.97	2.02	1.44	1.01	0.73	0.51	0.39
±68	16	=	1	×	16	3.03	1.84	1.29	0.92	0.70	0.46	0.33	0.24
±34	32	=	2	×	16	2.61	1.81	1.27	0.89	0.62	0.45	0.32	0.23
±17	64	=	4	×	16	1.66	1.13	0.80	0.56	0.41	0.29	0.20	0.14
±8	128	=	8	×	16	1.13	0.77	0.55	0.38	0.28	0.19	0.14	0.10

Table6.9-4(b) SD18 RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024}(\text{ADO}[k] - \text{Average})^2}\right) \Big/ 2^{23}$$

$$\text{Where FSR (Full - Scale Range)} = 2 \times \text{VREF/Gain.}$$

$$\text{Average} = \frac{\sum_{k=1}^{1024}(\text{ADO}[k])}{1024}$$

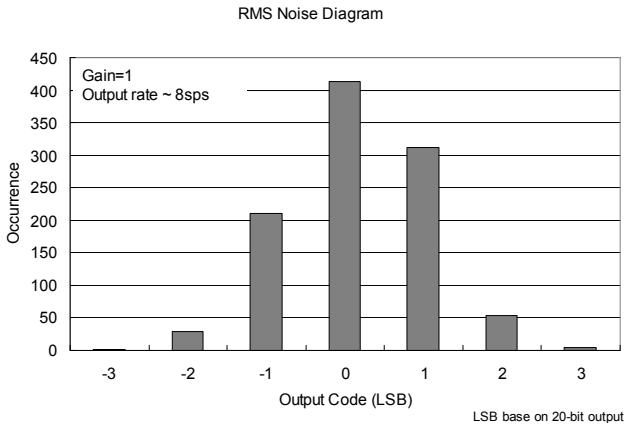


Figure6.9-4(a) RMS Noise Diagram

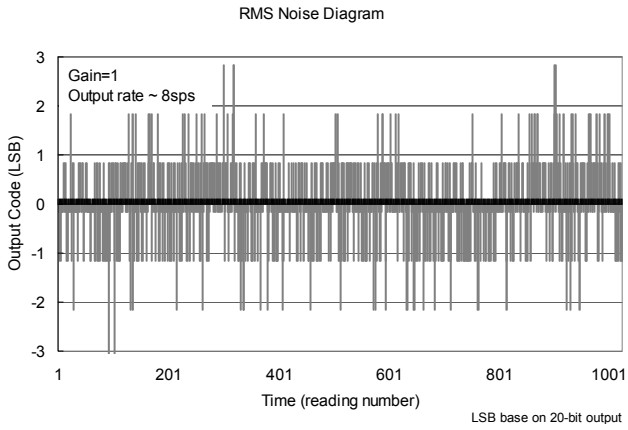


Figure6.9-4(b) Output Code Diagram

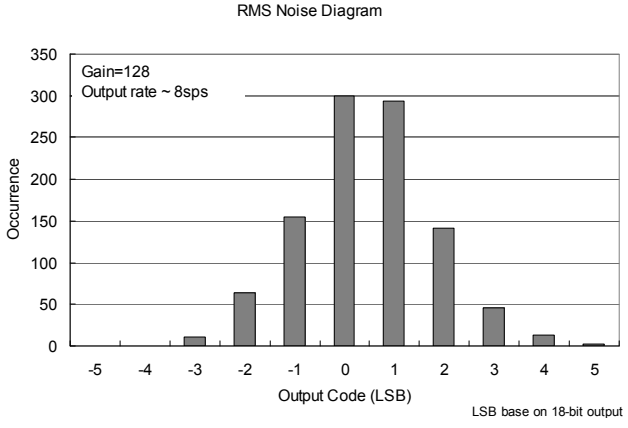


Figure6.9-4(c) RMS Noise Diagram

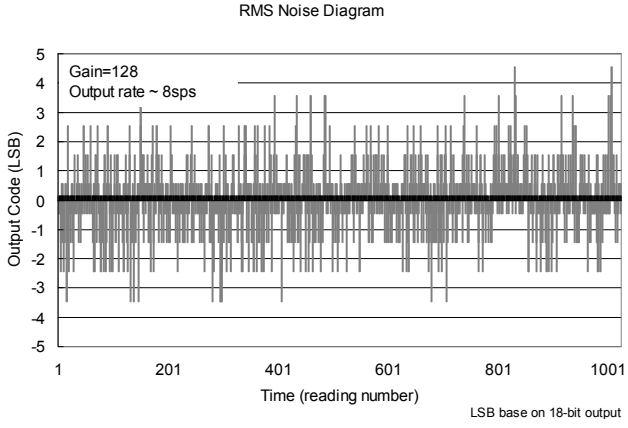


Figure6.9-4(d) Output Code Diagram

7. 訂貨資訊

下單品名[1]	封裝型式	引腳數	封裝型式描述方式		程式碼編號[2]	出貨包裝形式	個裝數量	材料組成	MSL[3]
HY11P14-D000	Die	-	D	000	000	-	100	Green[4]	-
HY11P14-L100	LQFP	100	L	100	000	Tray	90	Green[4]	MSL-3
HY11P14-L064	LQFP	64	L	064	000	Tray	250	Green[4]	MSL-3

[1] **產品名稱 – 封裝型式描述方式 – 程式碼編號（空白片 / 標準品 / 代客燒錄碼）**

例如：您的代客燒錄服務申請的程式碼編號為 008，且需要的產品是裸片出貨。則下單品名為HY11P14-D000-008

例如：您的需求是不帶程式碼的空白片且需要的產品是裸片出貨。則下單品名為HY11P14-D000

例如：您的需求是不帶程式碼的空白片且需要的產品是封裝片LQFP100 出貨，則下單品名為HY11P14-L100，且需以Tray出貨，則除下單品名外，請特別註明出貨包裝形式為Tray

例如：您的代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片LQFP100 出貨，則下單品名為HY11P14-L100-009，且需以Tray出貨，則除下單品名外，請特別註明出貨包裝形式為Tray

[2] **程式碼編號**

“001”~“999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

[3] **MSL:**

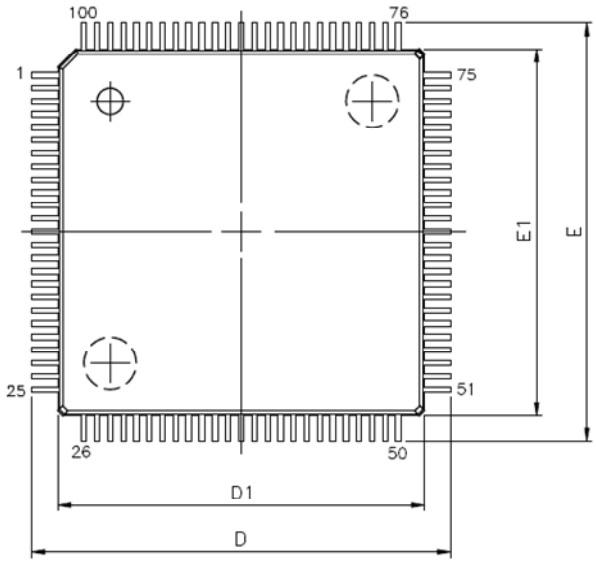
濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

[4] **Green (RoHS & no Cl/Br):**

HYCON產品皆為Green Product，符合RoHS 指令以及無鹵素規定(Br/Cl<0.1%)

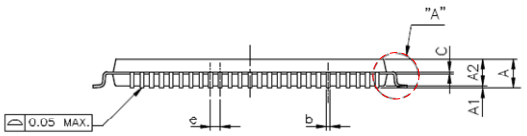
8. 封裝型式資訊

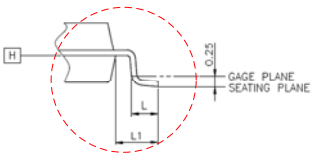
8.1 LQFP100(L100)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

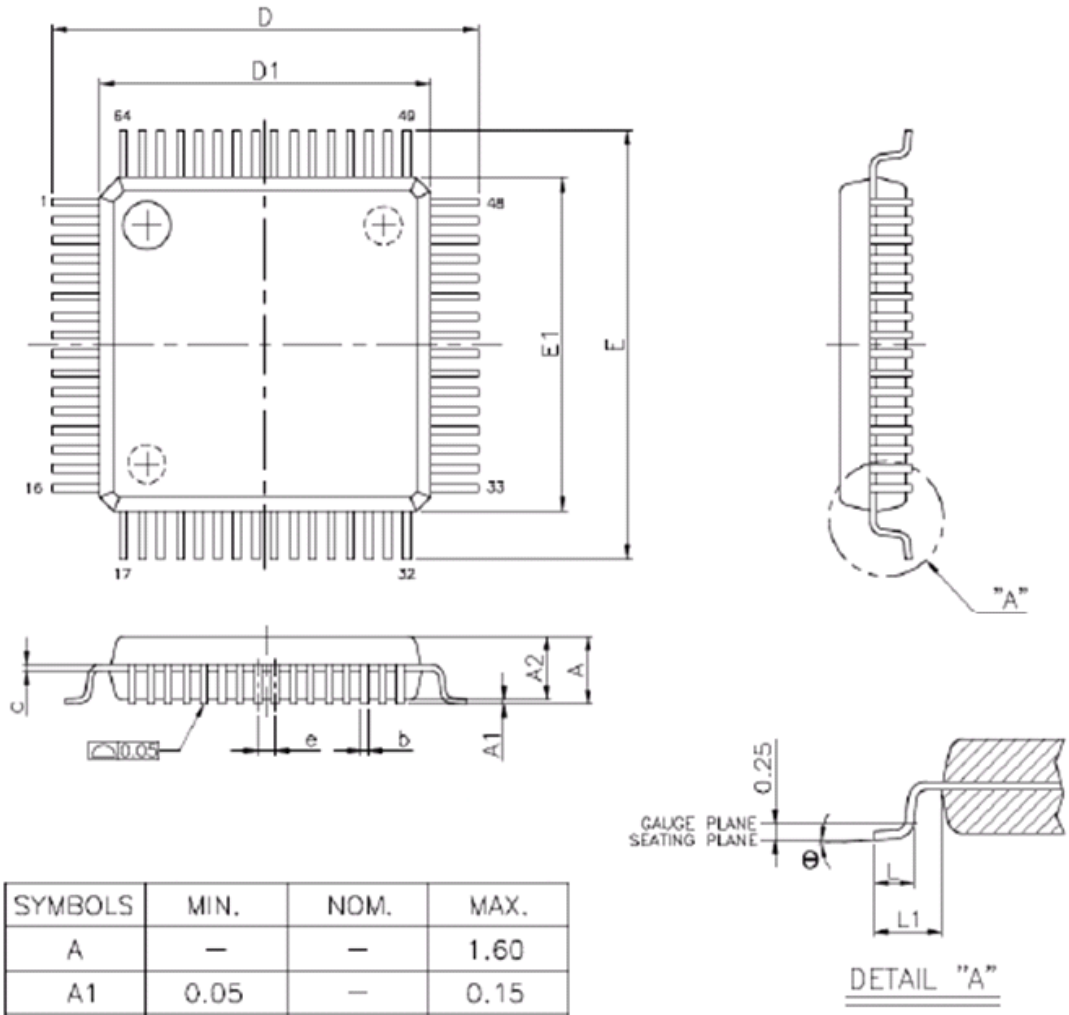




JEDEC MS-026 compliant

8.2 LQFP64(L064)

Unit :mm



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.

9. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

版本	頁次	變更摘要
V01	ALL	初版發行
V02	ALL	全面變更內容
V03	4	修訂 1 章節；增加 增強型比較器 說明
	30	修訂 7 章節；轉為中文資訊且編修欄位與內容
	32	新增**錯誤! 找不到參照來源。**章節；文件修訂記錄
V04	4	修訂 68 個指令成 67 個指令，特點內容修改
	6, 9	文字內容修改，增加PWM1/PWM2/PWM3 引腳說明
	13	增加PASC,PWMCN,PDBD暫存器說明
	22	Output voltage ,V_{ACM} 規格修改
	23	修改Figure6.6-5, Figure6.6-6
	25	Input offset voltage temperature drift.規格修改
	26	增加G_{SD18}Temperature Drift內容說明
V05	6~9	修訂章節內容
	11	修訂電路圖內容
	22~23	修訂章節內容
	26~28	修訂章節內容
V06	13	修訂章節內容
V07	4	修訂特點內容
	6	修訂I/O引腳定義內容
	22~23	修訂章節內容
V08	4	修訂特點內容
	22~23	修訂章節內容
V09	1	修訂封面格式
	4	修訂特點內容，刪除 1/2bias說明
	5	增加註 3 內容說明
	11	修訂應用電路圖，增加RST的RC電路
	20	刪除Detect V_{DD} voltage error內容說明
V10	11	修訂圖 3-1 腳位數字
	12	修增加圖 4-1 PORT PT3 說明
	13	增加SD18 Network章節
	23	修訂Power System溫飄規格
	30~31	增加SD18 Noise Performance章節
V11	4	修改 1.特點內容

	16	修改 6.電氣規格內容
	32	修改RMS Noise Diagram
V12	12	修改開發工具相關使用說明書編號
	13	修改圖 4-2 INH/INL
	24	修改圖片背景顏色
	33	增加訂貨資訊內容
V13	25	更新I_{LCD}電流規格
V14	14	增加Low Noise OPAMP Network
	15	增加Enhance Comparator Network
V15	All	增加LQFP64 封裝資料